**Future Tactical Radio Systems 2:15 pm - 5:15 pm 30 October 2001**
**Session C19:** *Joint Tactical Radio System Architecture*
**Chairs:** Col. Michael Cox, Steve Prewitt, Dr. Stephen Moore

# Digital RF Architectures for JTRS-Compliant Base-Stations

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# Overview

- Technology & Products
  - Digital RF Transceiver
    - True Software Radio
- Example benefits to JTRS platforms
  - 1. Co-Site Interference Mitigation
  - 2. HPA Linearization / Efficiency Enhancement
  - 3. Digital de-hopping of Link 16
  - 4. Increased hop rate for Wideband Network Waveform
  - 5. Increased link margins for Demand Assigned Multiple Access
  - 6. Massively Time Multiplexed DSP engines
- Enablers
  - Superconductor Digital IC Infrastructure Complete
    - Proof-of-Concept Established
  - Cryocooler Options Available

# Superconductor Digital Transceivers

- **Unique Capabilities**
  - Wideband High-fidelity data converters (ADC, DAC)
  - TeraOPS Digital Signal Processing (DSP)
- **Benefits**
  - Low-noise, high sensitivity receivers
  - Low-distortion, high efficiency broadband transmitters
- **Novel Architectures**
  - Direct Conversion at RF
  - Dynamically programmable hardware
  - Functions reconfigurable in software

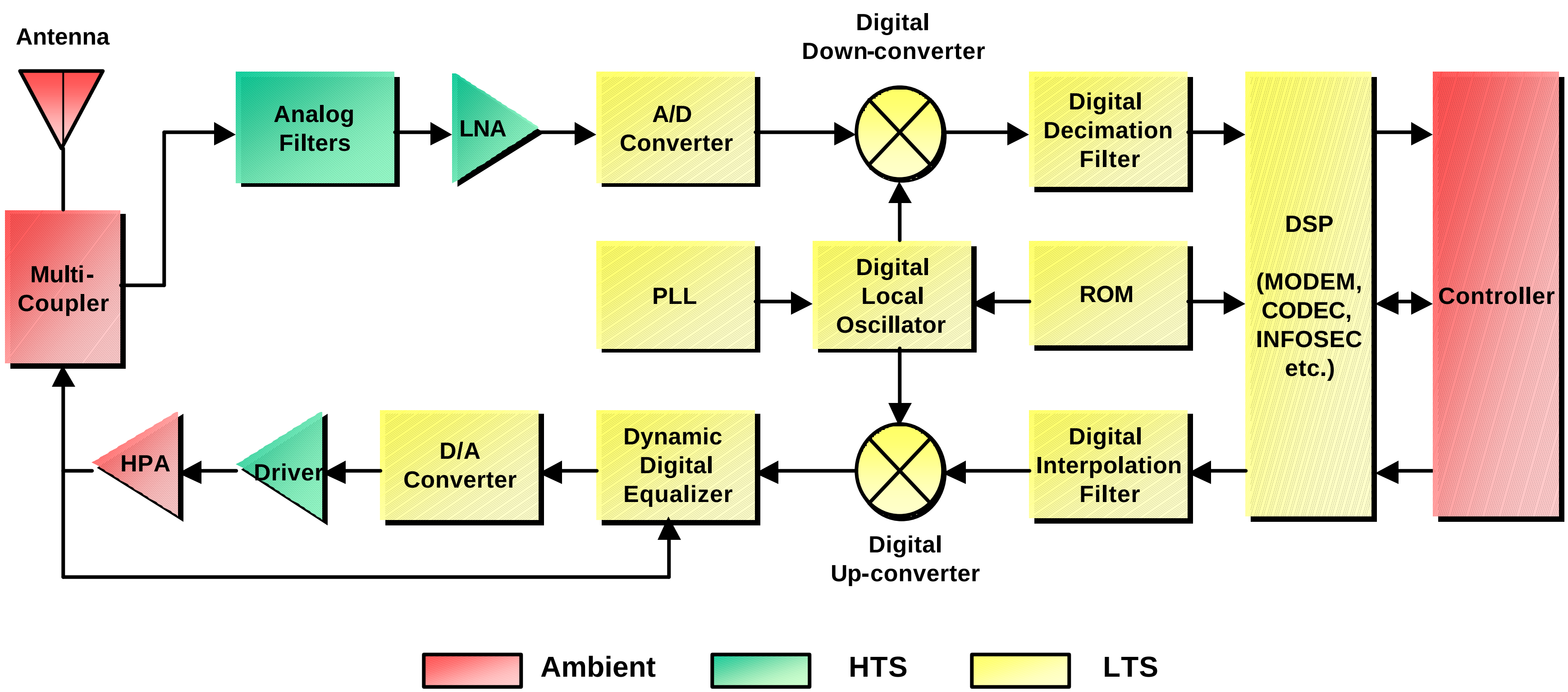
# Definition of "Software Radio"

"A **software defined radio** is defined as a radio in which the receive **digitization is performed at some stage downstream** from the antenna, typically after wideband filtering, low noise amplification, and down conversion to a lower frequency in subsequent stages, with a reverse process occurring for the transmit digitization. As technology progresses, a software defined radio can move to an almost **total software radio** where the **digitization is at the antenna** and all of the processing is performed by software residing in high-speed digital signal processors. The <u>software defined radio</u> will occur in the <u>near term</u> migrating to the <u>software radio</u> in the <u>longer term</u> subject to the <u>progression of core technologies</u>."

- SDR Forum

- **Employing a "software radio" architecture may be the only way to achieve the JTRS program objectives**
  - **8x waveforms**
  - **Legacy compatible**
  - **Future waveforms**

# True "Software Radio" Transceiver





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# Relevance to JTRS Cluster 1 Objectives

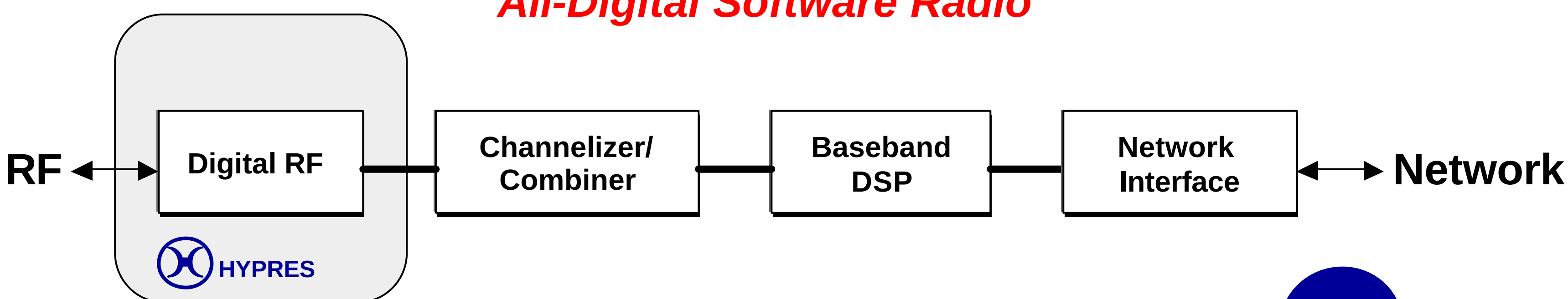
| Requirement | Objective | Superconductor Digital RF Approach | Technical Risk | Schedule Risk | Cost Risk |
|---|---|---|---|---|---|
| *Interoperability* | *100% IERs +commercial* | *Exceeds* | *Low* | *Low* | *Low* |
| *Network Ext. Coverage* | *Across Org. Boundaries* | *Enables* | *Low* | *Low* | *Low* |
| *Scalable* | *Maritime and Fixed* | *Exceeds* | *Low* | *Low* | *Low* |
| *Support Waveforms* | *All future WF's* | *Enables* | *Low* | *Moderate* | *Low* |
| *Simul. Chan. Operation* | *Veh:8+GPS Air:10+GPS* | *Exceeds* | *Low* | *Low* | *Low* |
| *Route & Retransmit* | *All WF's* | *Enables* | *Low* | *Low* | *Low* |
| *Software Configuration* | *Operator Load/Config* | *Enables* | *Low* | *Moderate* | *Low* |
| *Operational Availability* | *Ao = 0.99* | *Exceeds* | *Low* | *Low* | *Low* |
| *Internal Growth* | *Open Sys. Architecture* | *Enables* | *Low* | *Low* | *Low* |
| *Operating Frequency* | *2 MHz to 2 GHz* | *100 kHz to 2 GHz+* | *Low* | *Low* | *Low* |
| *Co-Site Interference* | *External devices* | *Exceeds Inherent in design* | *Low* | *Low* | *Low* |
| *Physical Size in Cu.In* | *Ground: 2160 Air LRU: 1080* | *Ground: <1500 Air LRU: <1000* | *Moderate (HPA size)* | *Low* | *Low* |
| *Weight in LB's* | *Ground: 83 Air LRU: 20* | *Ground: <40 Air LRU: <20* | *Moderate (HPA size)* | *Low* | *Low* |
| *Power* | *Not exceed legacy Sys.* | *< 75% of Legacy Sys.* | *Low* | *Low* | *Low* |

# HYPRES Digital RF Approach

***Direct***
***Sampling and Synthesis***
***at RF***

- **The *only* product that can provide direct conversion between RF and Digital Baseband Signals**
  - **with unprecedented bandwidth, resolution, fidelity, and sensitivity**
  - **orders of magnitude improved performance over any current or forecasted product**

***Enables the highly desired, but previously unattainable,***
***All-Digital Software Radio***

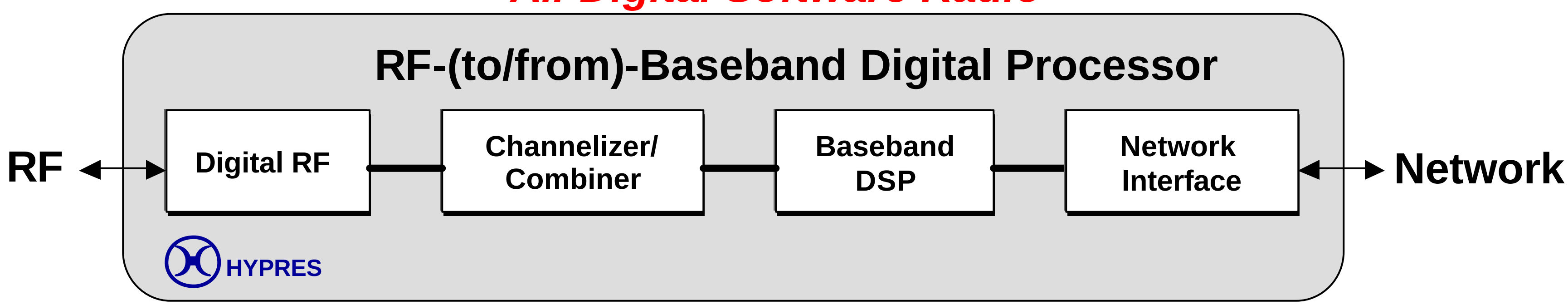


# Complete Digital RF Transceiver

***Complete RF-(to/from)-Baseband Digital Processor***

- **Total functionality of a base station in a single product,**
  excluding power amplifiers, antenna/tower, and standard ancillary equipment.

***Enables the highly desired, but previously unattainable,***
***All-Digital Software Radio***

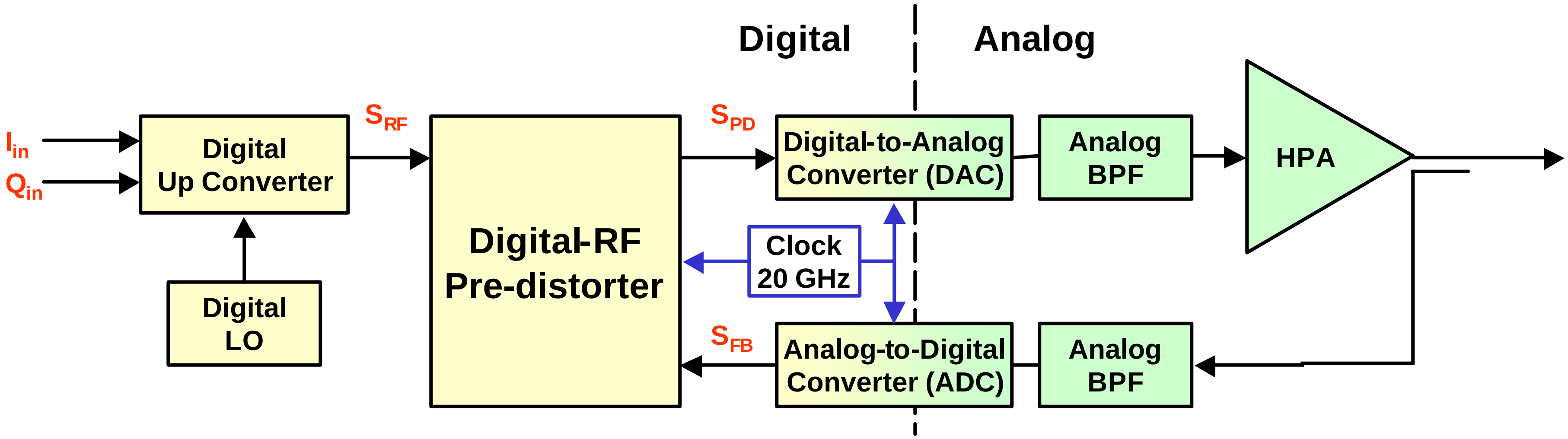


# 1. Co-Site Interference Mitigation

- Co-Site Interference has three main forms:
  - Small signal of interest in the presence of large interfering signal
  - Small signal of interest in the presence of a large number of equal strength signals
  - Impulsive interference from hoppers

**Solution:**
**High-SFDR ADC Front-end followed by Correlation-based Digital Signal Processing**

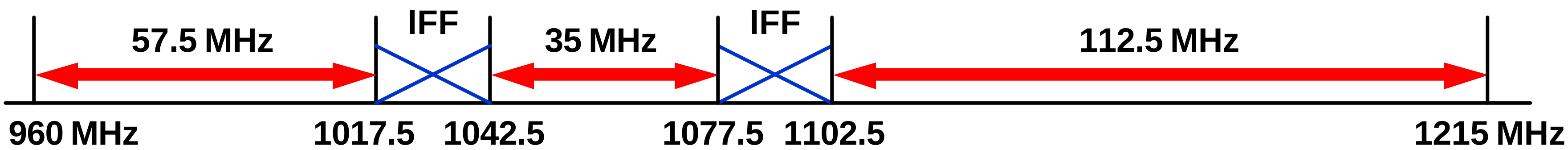
# 2. Power Amplifier Linearization




- ❑ Near real-time true digital Adaptive Linearization at RF
- ❑ Unparalleled High Dynamic Range & Bandwidth
- ❑ Frequency (& Data Rate) independent to >0.2 Clock Rate
- ❑ Efficiency enhancement up to the inherent limit of the HPA

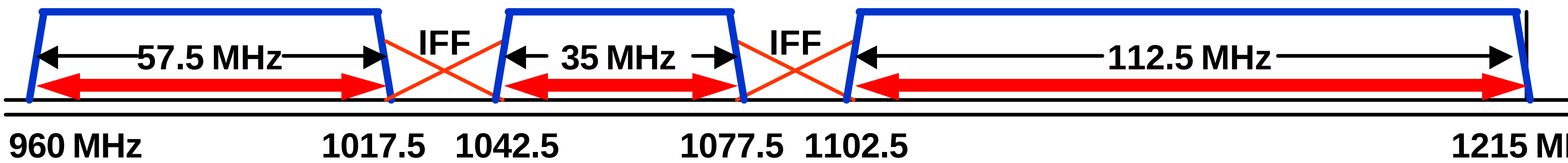
***One HPA covers Wide Bandwidths Consuming Less Power***

# 3. Digitally De-hopping Link-16




- Hopping occurs between 51 bands, each 3 MHz wide
- Present systems use “mode-selectable” hardware
- JTIDS bands overlap TACAN/IFF bands (at 1030 & 1090 MHz)
  - Interference with large TACAN signals are often severe ? High SFDR is essential.
- Systems with this specialized hardware configuration are not compatible with other radio waveforms and systems

# HYPRES Link-16 Solution: Digitization at RF

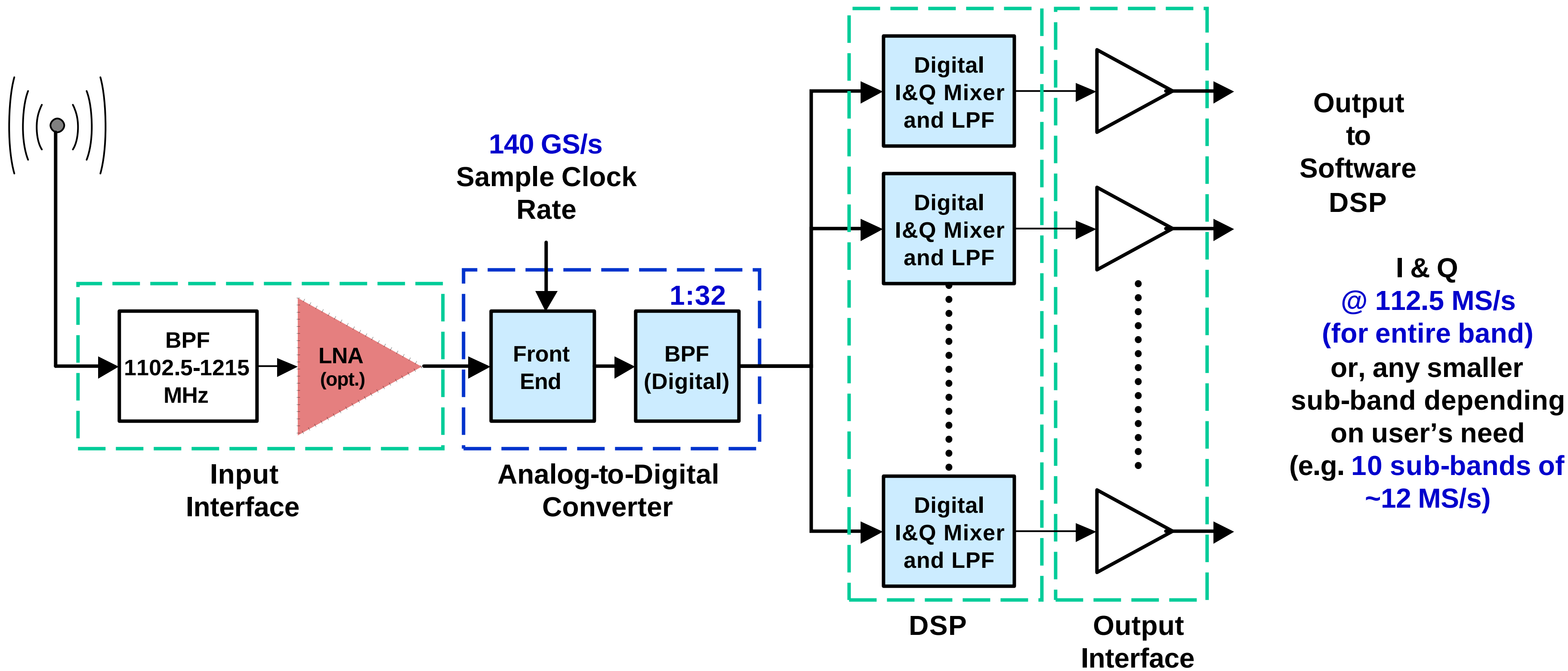



- The Link-16 band is broken up into 3 bands:
  - 960 – 1017.5 MHz (14 sub-bands of 3 MHz each)
  - 1042.5 – 1077.5 MHz ( 5 sub-bands of 3 MHz each)
  - 1102.5 – 1215 MHz (32 sub-bands of 3 MHz each)
- Directly digitize each band
- Produce digital I&Q outputs of each of the three bands or any set of sub-bands
  - 16 (4+2+10) sub-bands of ~12 MHz each that can be further processed in software

# Example HYPRES Band-pass ADC Architecture

**Input**

**1102.5-1215 MHz, 112.5-MHz-wide upper Link-16 band**




**Output**

**12-16 ENOB (>100 dB SFDR) Digital I & Q data in required format at 3-112.5 MS/s each**

# 4. Wideband Network Waveform (WNW)

## ❑ TOC-to-TOC Ultrahigh Bandwidth

- **Shaped Antenna Pattern for LPI/LPD**
  - Also solves Co-Site problem
- **WNW extensions for Anti-Jam**
- **Extend hop rate beyond that possible with conventional up-converter**
- **Hop rate attainable only with Digital RF**
  - Access Control by physics
  - Chip energy spread outside of normal bands
  - Baseband Synthesis techniques at RF rates
- **RF Fingerprint Masking**
  - Ability to “jitter” amplifier characteristics
  - Almost impossible to do with analog uplink

**- Interference Mitigation**

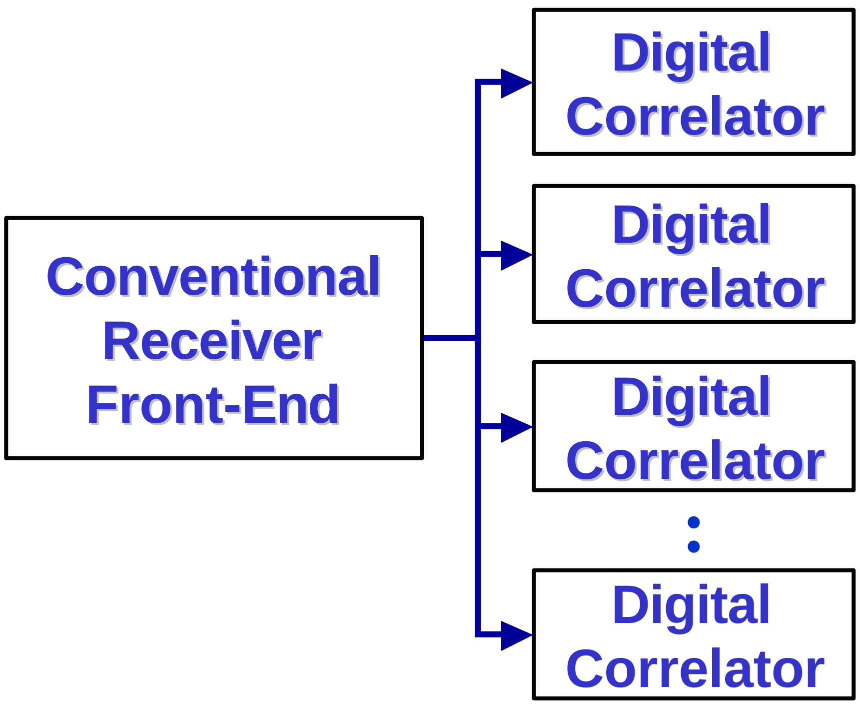
- RF output clean of intermodulation products

# 5. Increasing DAMA Link Margins

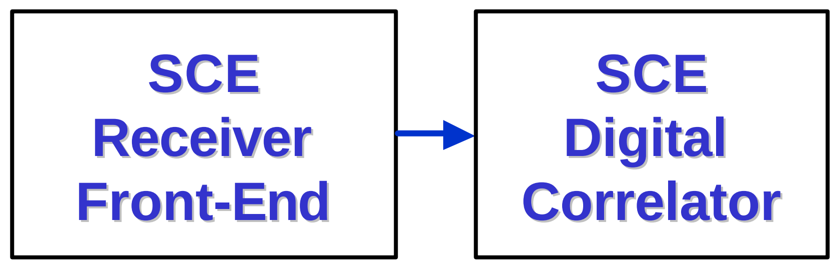
- **Narrowband Demand Assigned Multiple Access (DAMA) compromised by poor Link Margins**
  - **Digital RF sensitivity eliminates LNA**
  - **Current state-of-the-art suffers $5^+$ dB Loss**
  - **Digital RF offers**
    - Additional 2 dB uplink margin
      - Transponder pre-Distortion
    - Additional 3 dB downlink margin
      - Packetized demodulation
  - **JTRS Cluster One Appendix Requires 1.5 dB loss**

# 6. Massively Time-Multiplexed Processing

- Conventional Processing
- Slow, Parallel Hardware




- Superconducting Electronics (SCE) Processing
- Fast, Serial Hardware
  - Time-sharing of tasks
  - Hardware re-use
  - Cost Saving

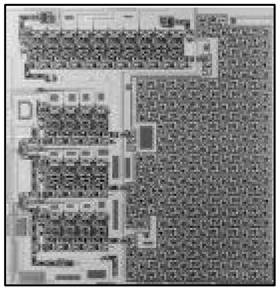



***Correlator becomes a matched Digital RF filter***

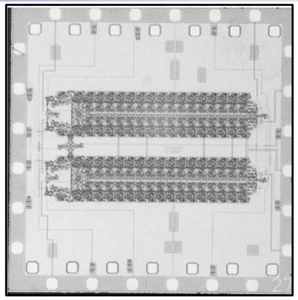
# Superconductor Back-End Processors

- ❑ **Superior speed of SCE can produce independent multi-Tera-Ops back-end digital signal processor products for conventional transceivers**
  - **Massively time-multiplexed correlation-based Walsh-Hadamard (WH) Demodulator — Large cost savings**
    - Separate WH Demodulators are now used for each multipath of each reverse link being processed by a base station (parallel processing)
    - Serialization of tasks using SCE processors provide hardware savings by more than an order of magnitude (serial processing)

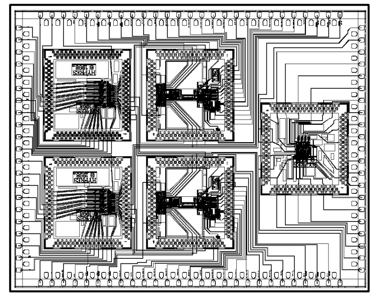
# HYPRES Superconductor IC Infrastructure



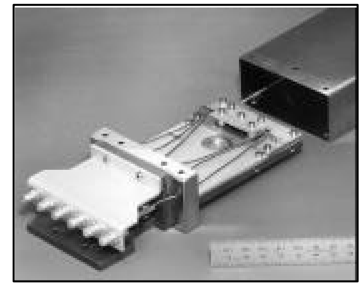
Digital-to-Analog Converters (DAC)



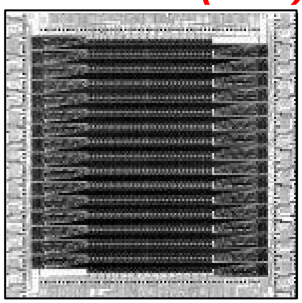
Fast Fourier Transforms (FFT)



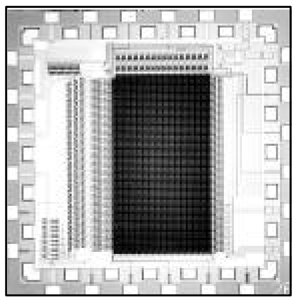
Multi-chip Module Packages (MCM)



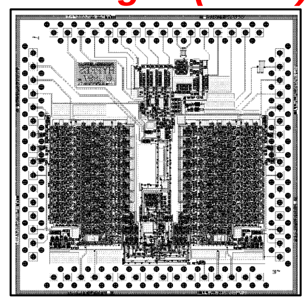
Optical I/O and Packaging



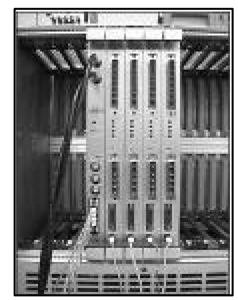
Network Swtiches



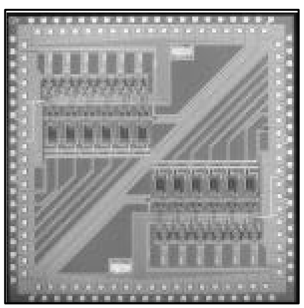
Random Access Memories (RAM)



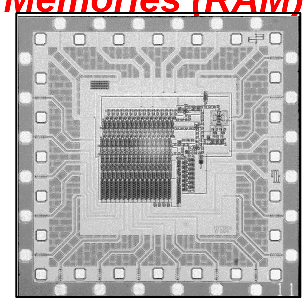
Digital I&Q Converters



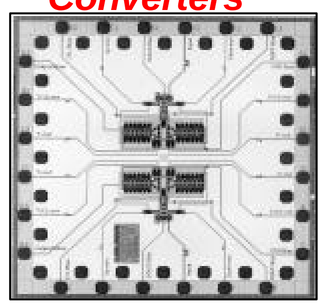
User Interfaces



Analog-to-Digital Converters (ADC)



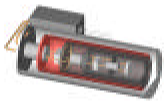
Digital Signal Processing (DSP)



Low-jitter Clocks and Phase-Locked Loops (PLL)

# Cryocooler Choices/Advantages

- **Key enablers of high performance, demonstrated in:**
  - Wireless cellular communications (HTS filters)
  - Mine detection
  - Highest sensitivity radar receivers
  - IR imaging systems
- **Proven to meet any and all requirements as designed:**
  - Reliability (demonstrated MTBF of 40 years)
  - Ruggedness (proven in space environment)
  - Combat environment (proven in IR imaging systems)
  - Efficiency (MEMS package)
- **Multiple vendors (ready to perform) and approaches leading to competitive choices and selection:**
  - Commercial vendors (Leybold, Air Liquide)
  - Military contractors (Ball Aerospace, Lockheed Martin)
  - Small Business (TAI, Sunpower, Creare)

***Performance/Reliability exceeding JTRS Cluster 1 Requirements Assured***

# Conclusion

- JTRS performance objectives demand a true software radio approach
- A Superconductor Digital RF transceiver can enable such a software radio
  - Circuits and cryopackaging demonstrated
- Leads to straightforward solutions for complex issues including
  - Co-site interference
  - Distortions from non-linear high power amplifiers
  - Complex waveforms (DAMA, Link 16, WNW, etc.)
  - TeraOPS-level DSP

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